DATA SHEET

QSFP10-CSR4-C-GEN

40Gb/s QSFP+ SR4 Transceiver

QSFP10-CSR4-C-GEN Overview

QSFP10-CSR4-C-GEN QSFP+ SR4 optical transceivers are based on Ethernet IEEE P802.3ba standard and SFF 8436 standard. QSFP+ SR4 offers 4 independent transmit and receive channels, each capable of 10Gbps for an aggregate bandwidth of 40Gbps.

Product Features

- 4 high-speed full duplex channels
- Multi Rate, up to 10.5Gbps per channel
- QSFP+ MSA compliant
- Up to 300 meters over OM3 Multimode Fiber and 400 meters over OM4 Multimode Fiber.
- Low Power consumption, less than 1W
- Reliable VCSEL array technology
- Single 1X12 MPO receptacle
- RoHS Compliant
- With digital diagnostic monitoring functions
- Operating temperature range: 0°C to 70°C

Applications

- 40GBASE-SR4 40G Ethernet
- Breakout to four 10GBASE-SR Ethernet

Ordering Information

Part Number	Description	Color on Clasp
QSFP10-CSR4-C-GEN	40G QSFP+ 850nm MPO Connectors, Up to 300m on OM3 MMF and 400m on OM4 MMF	Cream color

For More Information:
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General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			10^{-12}		
Operating Temperature	T_C	0		70	°C	1
Storage Temperature	T_{STO}	-40		85	°C	2
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	3

Notes:
1. Case temperature
2. Ambient temperature
3. For electrical power interface

Optical – Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Output Optical Power (per lane)	P_{TX}	-7.6		2.4	dBm	
Optical Center Wavelength	λ_C	840		860	nm	
Extinction Ratio	ER	3			dB	
RMS Spectral Width	$\Delta\lambda$			0.45	nm	
Relative Intensity Noise	RIN			-128	dB/Hz	
Transmitter Dispersion Penalty	TDP			3.5	dB	
Transmitter Eye Mask						1
Launch Power of OFF Transmitter	P_{OUT_OFF}			-30	dBm	2

Notes:
1. Compliant with IEEE 802.3ba
2. Average

Optical – Characteristics – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Optical Center Wavelength	λ_C	840		860	nm	
Optical Input Power(per lane)	P_{RX}	-9.5		2.4	dBm	1
Damage Threshold	P	3.3			dBm	
Receiver Sensitivity (OMA)@10.3Gb/s	R_{X_SEN1}			-11.1	dBm	
Stressed Receiver Sensitivity in OMA, (per lane)				-7.5	dBm	
Receiver Reflectance	TR_{RX}			-12	dB	
LOS Assert	LOS_A	-25			dBm	
LOS De-Assert	LOS_D			-12	dBm	
LOS Hysteresis	LOS_H	0.5			dB	

Notes:
1. Average, Informative

Electrical – Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR			10.5	Gb/s	1
Differential data input swing	V_{IN_PP}	180		1200	mV	
Single Ended Input Voltage Tolerance	V	-0.3		3.8	mV	
Transmit Disable Voltage	V_D	V_{CC}-1.3		V_{CC}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		V_{EE}+0.8	V	

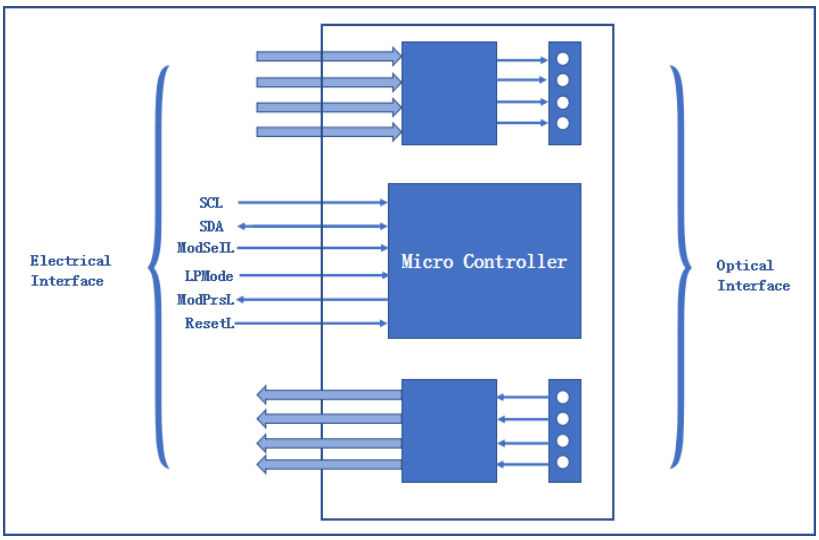
Notes:
1. Non-condensing

Electrical – Characteristics – Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR			10.5	Gb/s	
Differential Data Output Swing	V_{OUT_PP}	340		800	mV	
Differential Output Amplitude in Squelched state	V_{OUT_sq}			50	mV	
Single Ended Output Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{cm}			7.5	mV	1
Data Output Rise/Data Output Rise (20%-80%)	t_r/t_f	28			ps	
Total Jitter (p-p)	TJ			0.7	UI	
Deterministic Jitter (p-p)	DJ			0.4	UI	

Note:
1.RMS

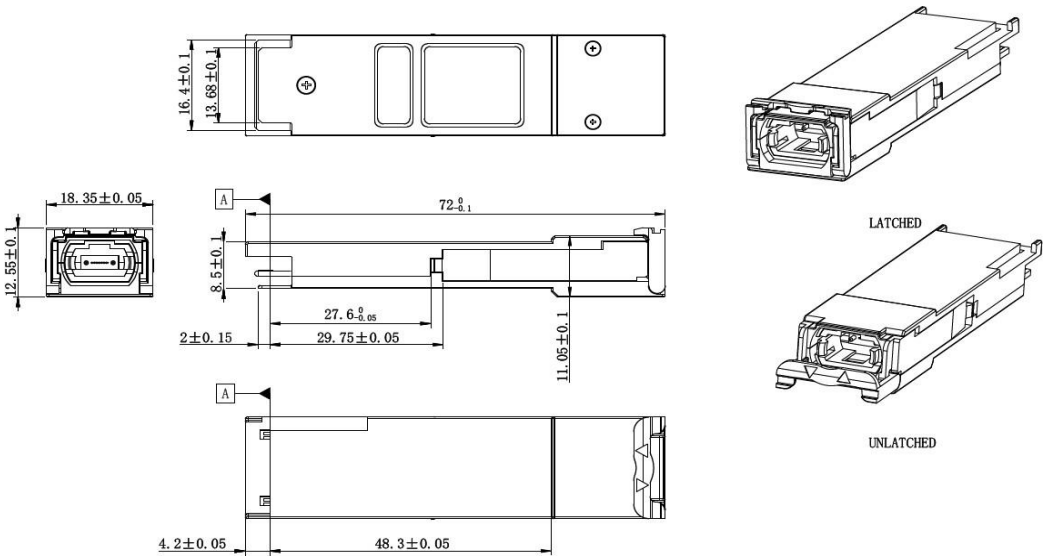
Block-Diagram-of-Transceiver



Functions Description

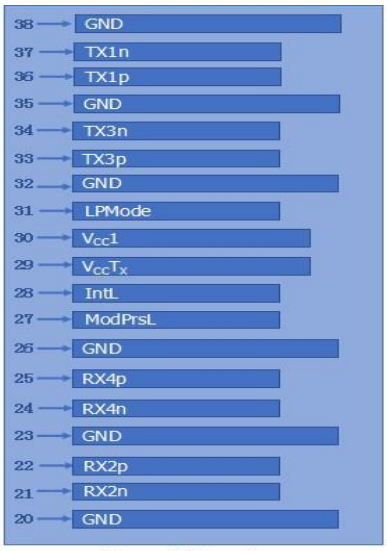
The QSFP-SR4 has miniature optical engine embedded into QSFP module. The engines interconnect 4 independent transmit/receive lanes.A functional block diagram of the engine is shown in the above Figure. The transmitter sections consist of a 4-channel VCSEL array, a 4-channel input buffer and laser driver. An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

Dimensions

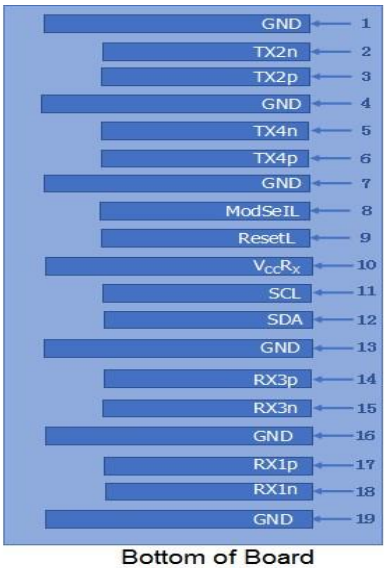


ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

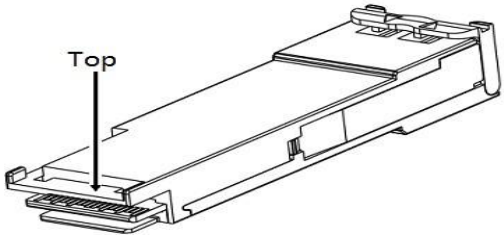
Electrical Pad Layout

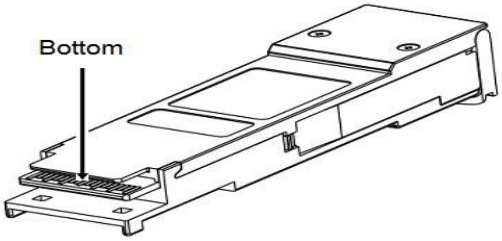


Top of Board



Bottom of Board





Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

33	Tx3p	Transmitter Non-Inverted Data Input, LAN3	
34	Tx3n	Transmitter Inverted Data Input, LAN3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, LAN1	
37	Tx1n	Transmitter Inverted Data Input, LAN1	
38	GND	Ground	5

Notes:
1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module
2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting
3. This pin is active high, indicating that the module is running under a low power module.
4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source
5.Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbps 4X PLUGGABLE TRANSCEIVER –SFF-8436.