DATA SHEET

AOC-QSFP28-2QSFP28-OM3-aaa.aaM

100G QSFP28 to two 50G QSFP28 Active Optical Cable

AOC-QSFP28-2QSFP28-OM3-aaa.aaM Overview

AOC-QSFP28-2QSFP28-OM3-aaa.aaM QSFP28 to 2x50G QSFP28 active optical cable are used for 100G QSFP28 to two 50G QSFP28 application. The full-duplex optical assembly offers 4 independent transmit and receive channels, each capable of up to 25Gbps for an aggregate bandwidth of 100Gbps.

QSFP28 AOC can be used as a direct replacement for traditional copper cables with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 70 meters.

Product Features

• Hot-pluggable QSFP28 form factor
• 4 high-speed full duplex channels
• Supports 103.1Gb/s aggregate bit rate
• 4x25Gbps 850nm VCSEL laser
• QSFP28 MSA compliant
• Low power dissipation:<2W per module
• Cable lengths from 1 to 70 meters
• RoHS-6 Compliant
• Operating temperature range: 0°C to70°C (Case temperature)

Applications

• 100G Ethernet
• Infiniband interconnects

Ordering Information

Part Number	Description	Color on Clasp
AOC-QSFP28-2QSFP28-OM3-aaa.aaM	100G QSFP28 Active Optical Cable (length from 1m to 70m, conventional fiber color is aqua green, color can be customized)	Beige
For More Information: SONGXIN TAIPEI TECH SOLUTIONS CO., LTD. Web: www.songxin.com.tw Email: oversea@songxin.com.tw		

General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	BER			5×10^{-5}		1
Bit Error Rate	BER			1×10^{-12}		2
Operating Temperature	T_C	0		70	$^\circ$C	3
Storage Temperature	T_{STO}	-40		85	$^\circ$C	4
Input Voltage	V_{CC}	3.14	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	5
Minimum bending radius	R	30			mm	

Notes:
1. Tested using the pseudo-random code PBRS31
2. Need to use forward error correction code FEC
3. Case temperature
4. Ambient temperature
5. For electrical power interface

AOC Electrical Input Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR	25.78±100ppm			Gb/s	1
Differential Input Amplitude	V_{IN_PP}	180		1200	mV	
Differential Input Impedance	Z_{in}	90	100	110	ohm	
Differential Return Loss	SDD22	Per OIF CEI-28G-VSR and CAUI-4 requirements			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion	SDC22, SCD22				dB	
Transition Time(20%-80%)	t_r/ t_f	10			ps	

Notes:
1. By switching CDR, our QSFP28 AOC can support different data rate

AOC Electrical Output Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR	25.78±100ppm			Gb/s	1
Differential Output Amplitude	V_{OUT_PP}	400	600	800	mV	
Differential Onput Impedance	Z_{out}	90	100	110	ohm	
Differential Return Loss	SDD22	Per OIF CEI-28G-VSR and CAUI-4 requirements			dB	
Common Mode to Differential conversion and Differential to Common Mode conversion	SDC22, SCD22				dB	
Transition Time (20%-80%)	t_r/ t_f	9.5			ps	

Notes:
1. By switching CDR, our QSFP28 AOC can support different data rate

## Block-Diagram-of-Transceiver
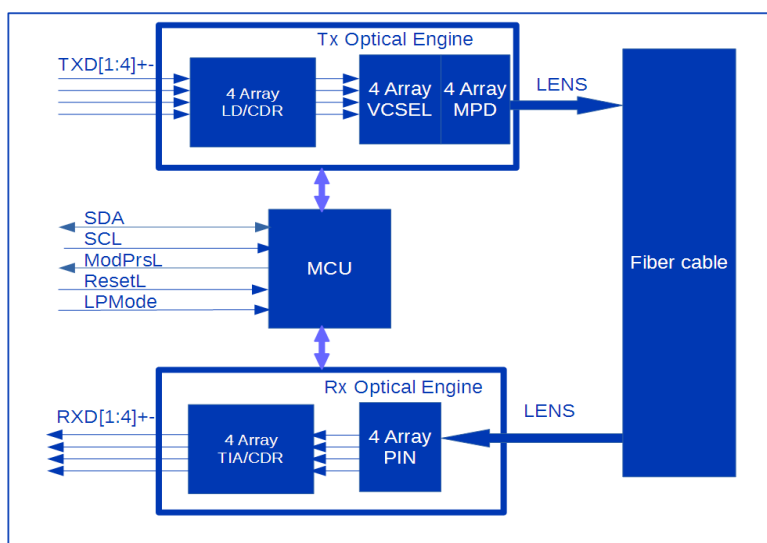
Functions Description

AOC-QSFP28-2QSFP28 is manufactured using the advanced COB (Chip on Board) process. It consists of a microcontroller, a transmitter optical engine and a receiver optical engine. The AOC has built-in clock and data recovery functions. The default 4 channels are fixed at 25.78Gbps rate range. Modify the settings. The module can also work in the 28Gbps range and support OTN services. If you need other speed range versions or dual rate range versions, you can contact us for special customization.

The transmitter optical engine includes a 4-channel transmitter clock data recovery (CDR) and laser driver circuit (LD), a 4-channel VCSEL laser array, and a 4-channel detection photodiode (MPD) array. The high-speed differential electrical signal output by the host is sent to the laser driver for amplification by CDR recovery shaping, driving the VCSEL laser to generate an optical signal, and the optical signal is coupled to the optical fiber through the optical lens. The light engine integrates a photodiode for detection for output optical power detection, and the laser driver uses an automatic optical power control loop to ensure the stability of the transmitted optical power.

The receiver optical engine includes a 4-channel photodiode (PIN) array, a 4-channel signal amplifier (TIA/LA) and a receiver-side clock data recovery circuit (CDR) array. The optical signal in the fiber is coupled to a receiving photodiode (PIN) through an optical lens to convert it into a photocurrent.T he photo-generated current signal is amplified by the amplifier, sent to the CDR circuit and recovered from the clock and data signals, and finally output to the host as a high-speed differential signal.

The microcontroller communicates with the host via a 2-wire serial communication interface, providing module control, status reporting and monitoring (DOM). This product complies with the SFF-8636 standard. This product complies with the requirements of the IEEE 802.3bm standard. With the support of RS-FEC, it can reach a transmission distance of 70 meters in OM3 fiber.

Fan-out Block Diagram of 100G QSFP28 to 2X50G QSFP28 Active optical cable
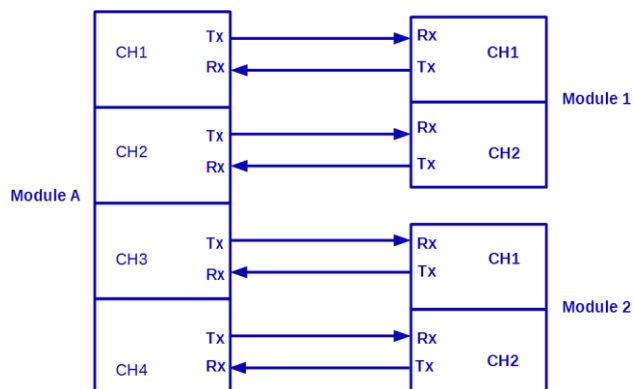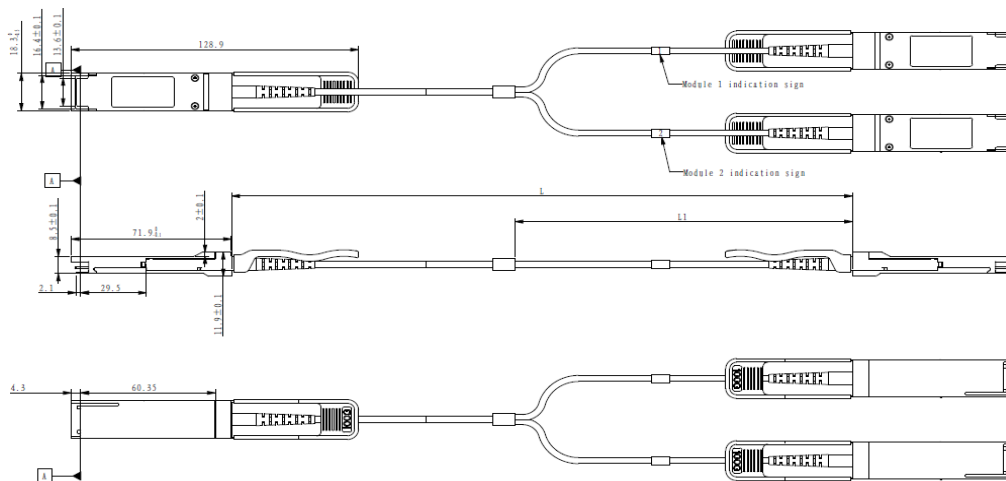
Notes:
Module 1 has an indication sign "1" on the fiber cable
Module 2 has an indication sign "2" on the fiber cable
Module A has no indication sign

Dimensions

ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED
UNIT: mm

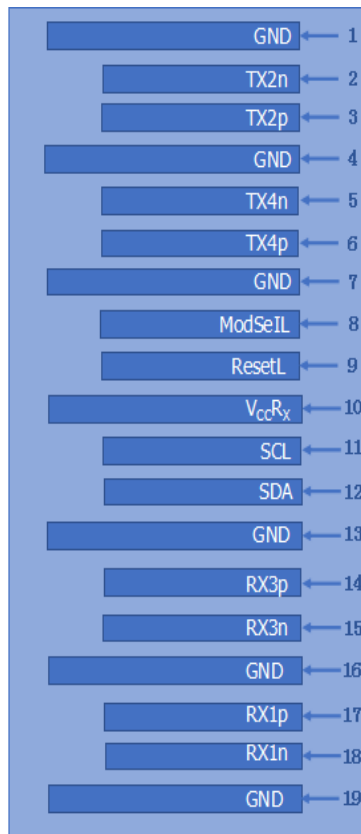| Cable length(meter)	L(meter)	L1(meter)
1	1	0.67
2	2	1.33
3	3	2
5	5	3
7	7	3
10	10	3
15	15	3
20	20	3
30	30	3

Notes:
Branch length L1 can be customized according to customer requirements

Electrical Pad Layout

	Top of Board		Bottom of Board	
38 →	GND		GND ←	1
37 →	TX1n		TX2n ←	2
36 →	TX1p		TX2p ←	3
35 →	GND		GND ←	4
34 →	TX3n		TX4n ←	5
33 →	TX3p		TX4p ←	6
32 →	GND		GND ←	7
31 →	LPMode		ModSeIL ←	8
30 →	$V_{cc}1$		ResetL ←	9
29 →	$V_{cc}T_X$		$V_{cc}R_X$ ←	10
28 →	IntL		SCL ←	11
27 →	ModPrsL		SDA ←	12
26 →	GND		GND ←	13
25 →	RX4p		RX3p ←	14
24 →	RX4n		RX3n ←	15
23 →	GND		GND ←	16
22 →	RX2p		RX1p ←	17
21 →	RX2n		RX1n ←	18
20 →	GND		GND ←	19
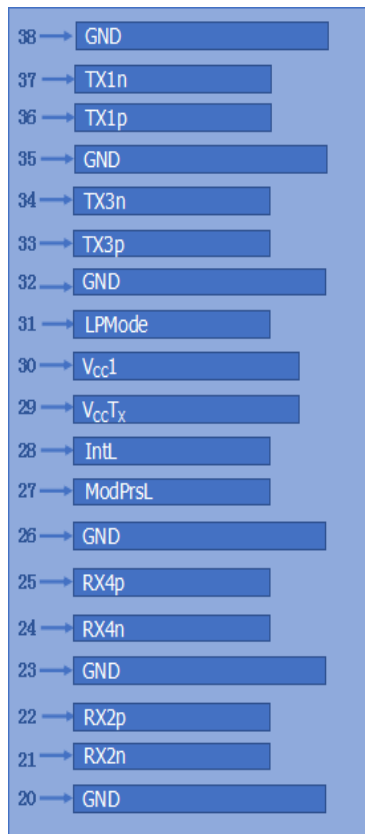
Top of Board **Bottom of Board**

Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	5
2	Tx2n	Transmitter Inverted Data Input, LAN2	
3	Tx2p	Transmitter Non-Inverted Data Input, LAN2	
4	GND	Ground	5
5	Tx4n	Transmitter Inverted Data Input, LAN4	
6	Tx4p	Transmitter Non-Inverted Data Input, LAN4	
7	GND	Ground	5
8	ModSelL	Module select pin, the module responds to two-wire serial communication when low level	1
9	ResetL	Module Reset	2
10	$V_{cc}R_X$	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	5
14	Rx3p	Receiver Non-Inverted Data Output, LAN3	
15	Rx3n	Receiver Inverted Data Output, LAN3	
16	GND	Ground	5
17	Rx1p	Receiver Non-Inverted Data Output, LAN1	
18	Rx1n	Receiver Inverted Data Output, LAN1	
19	GND	Ground	5
20	GND	Ground	5
21	Rx2n	Receiver Inverted Data Output, LAN2	
22	Rx2p	Receiver Non-Inverted Data Output, LAN2	
23	GND	Ground	5
24	Rx4n	Receiver Inverted Data Output, LAN4	
25	Rx4p	Receiver Non-Inverted Data Output, LAN4	
26	GND	Ground	5
27	ModPrsL	The module is inserted into the indicate pin and grounded in the module.	3
28	IntL	Interrupt	4
29	$V_{cc}T_X$	+3.3V Power Supply transmitter	
30	V_{cc1}	+3.3V Power Supply	
31	LPMode	Low Power Mode	5
32	GND	Ground	5

33	Tx3p	Transmitter Non-Inverted Data Input, LAN3	
34	Tx3n	Transmitter Inverted Data Input, LAN3	
35	GND	Ground	5
36	Tx1p	Transmitter Non-Inverted Data Input, LAN1	
37	Tx1n	Transmitter Inverted Data Input, LAN1	
38	GND	Ground	5

Notes:

1. ModSelL is the input pin. The module responds to 2-wire serial communication commands when it is held low by the host. ModSelL allows multiple QSFP modules to be used on a single 2-wire interface bus. If ModSelL is High, the module will not respond to any 2-wire interface communication from the host. ModSelL has internal pull-up resistors in the module

2. The module restart pin, when the low level on the ResetL pin lasts longer than the minimum pulse length, resets the module and restores all user modules to their default state. When performing reset device, the host should ignore all status bits. Until the module reset interrupt is completed, please note that during hot plugging, the module will issue this information to complete the reset interrupt without resetting

3. This pin is active high, indicating that the module is running under a low power module.

4. IntL is the output pin, which is the open collector output and must be pulled up to Vcc on the motherboard. When it is low, it indicates that the module may malfunction. The host uses a 2-wire serial interface to identify the interrupt source

5.Circuit ground is internally isolated from chassis ground.

References

1. IEEE standard 802.3bm. IEEE Standard Department. 2.

QSFP28 4X PLUGGABLE TRANSCEIVER –SFF-8665.

3. SFF-8636 Specification for Management Interface for Cabled Environments.